FIG. 1

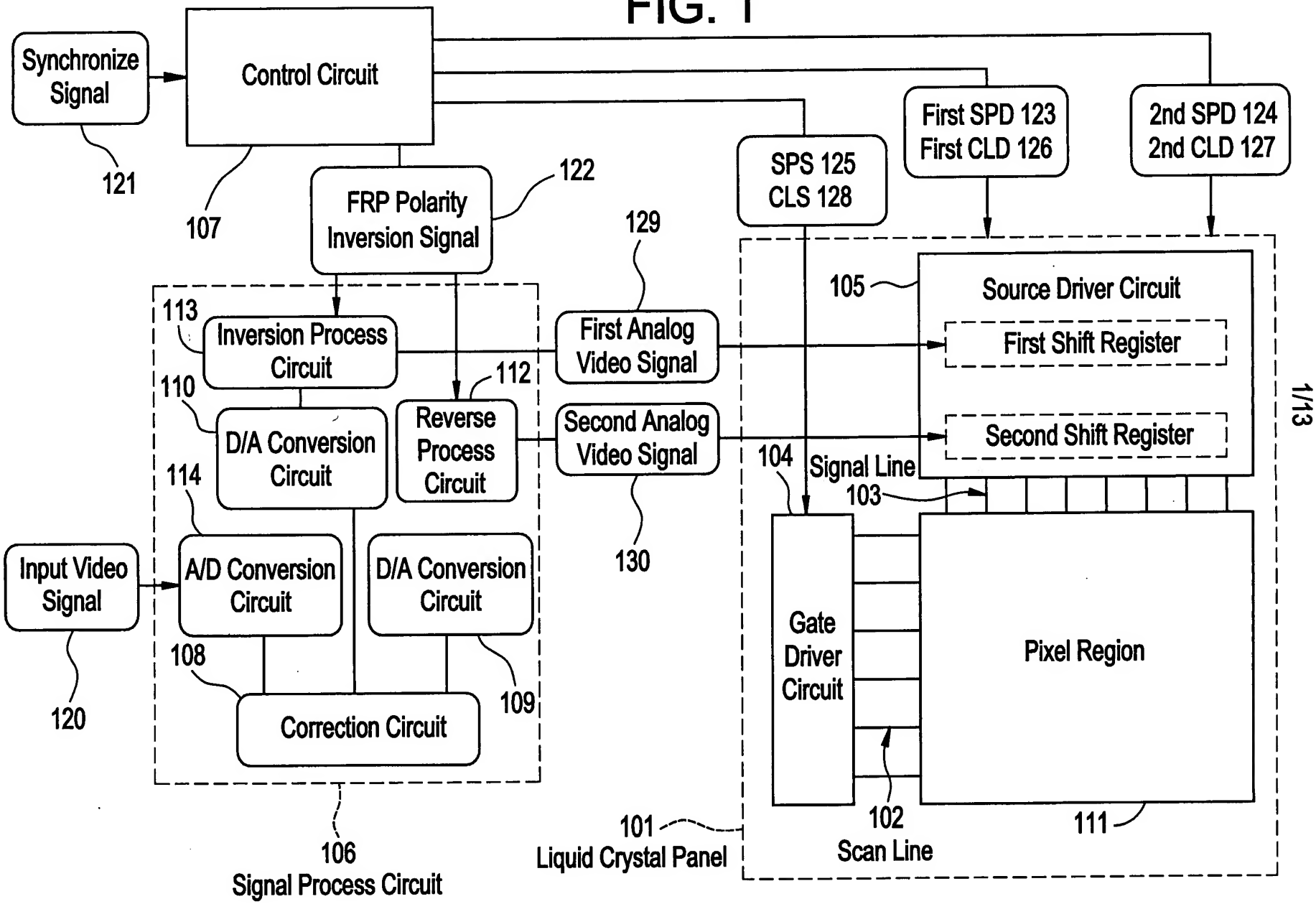

Synchronize Signal
121
Control Circuit
107
FRP Polarity Inversion Signal
122
SPS 125
CLS 128
First SPD 123
First CLD 126
2nd SPD 124
2nd CLD 127
129
105
Source Driver Circuit
First Shift Register
Second Shift Register
113
Inversion Process Circuit
110
D/A Conversion Circuit
112
Reverse Process Circuit
First Analog Video Signal
Second Analog Video Signal
130
104
Signal Line
103
114
A/D Conversion Circuit
D/A Conversion Circuit
Input Video Signal
120
108
109
Correction Circuit
Gate Driver Circuit
Pixel Region
102
Scan Line
111
101
Liquid Crystal Panel
106
Signal Process Circuit
1/13

FIG. 2A

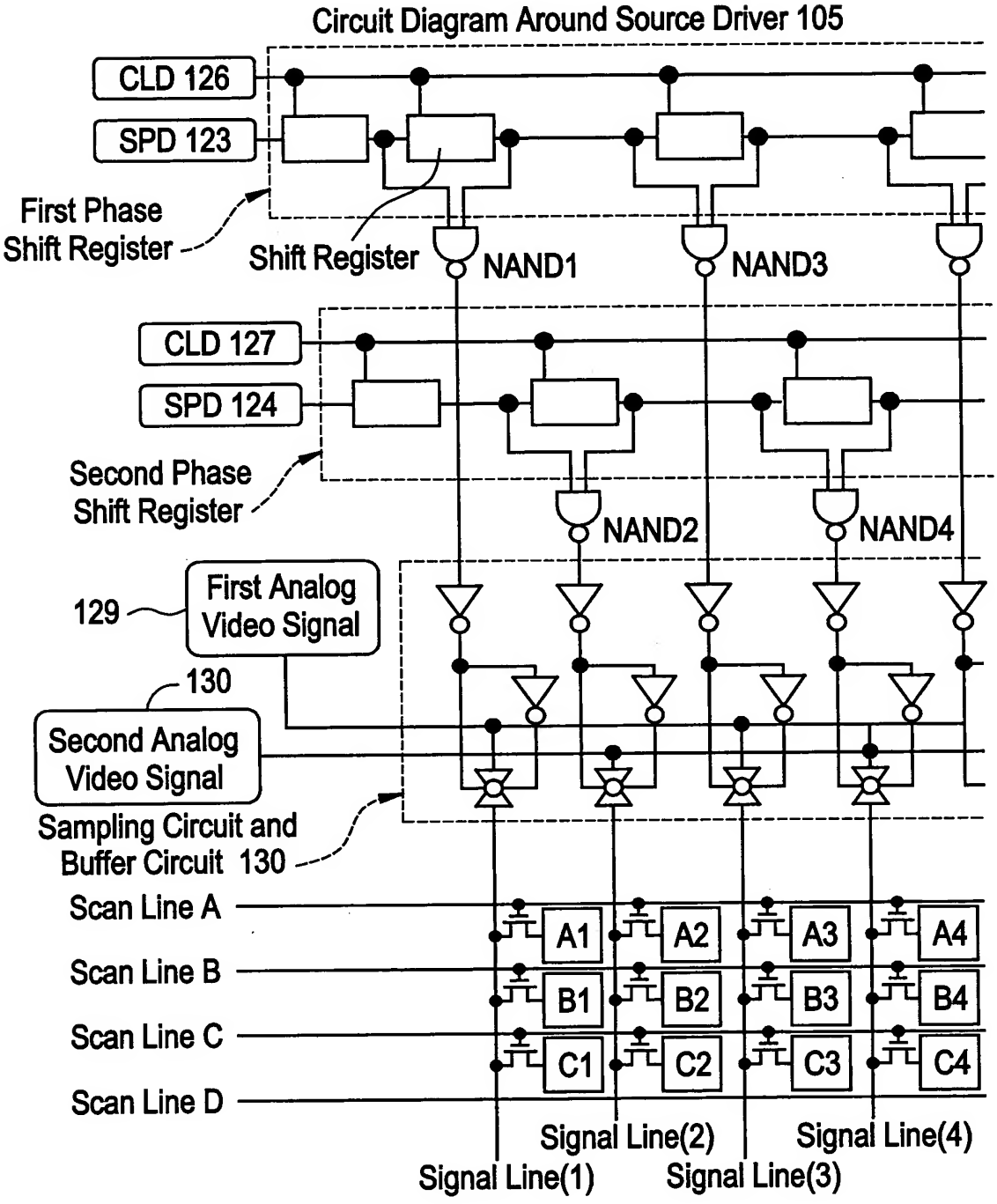


FIG. 2B

Display Pattern

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4

FIG. 3

Timing Chart of Source Driver Circuit

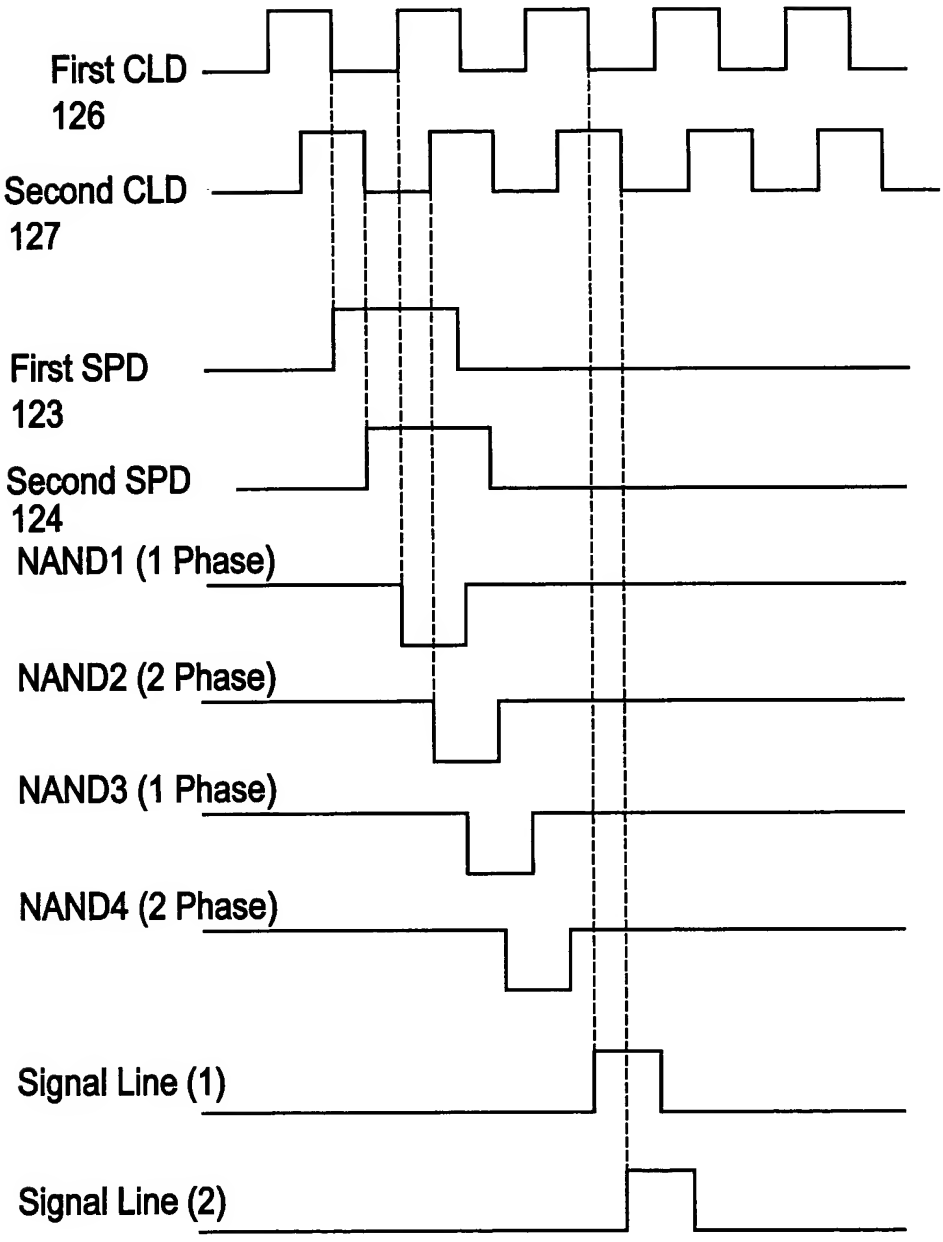


FIG. 4

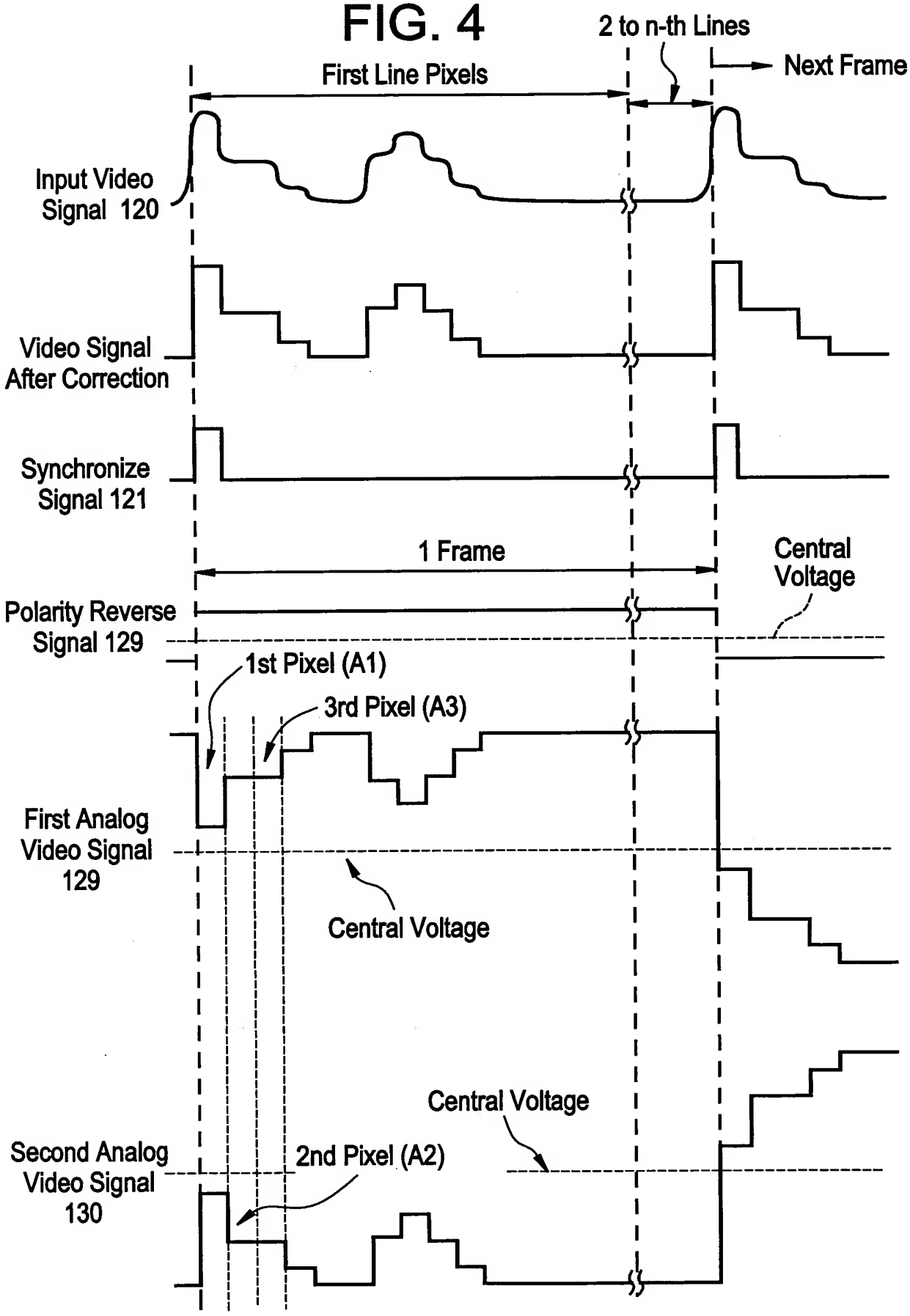

2 to n-th Lines
Next Frame
First Line Pixels
Input Video Signal 120
Video Signal After Correction
Synchronize Signal 121
1 Frame
Central Voltage
Polarity Reverse Signal 129
1st Pixel (A1)
3rd Pixel (A3)
First Analog Video Signal 129
Central Voltage
Central Voltage
Second Analog Video Signal 130
2nd Pixel (A2)

FIG.5A

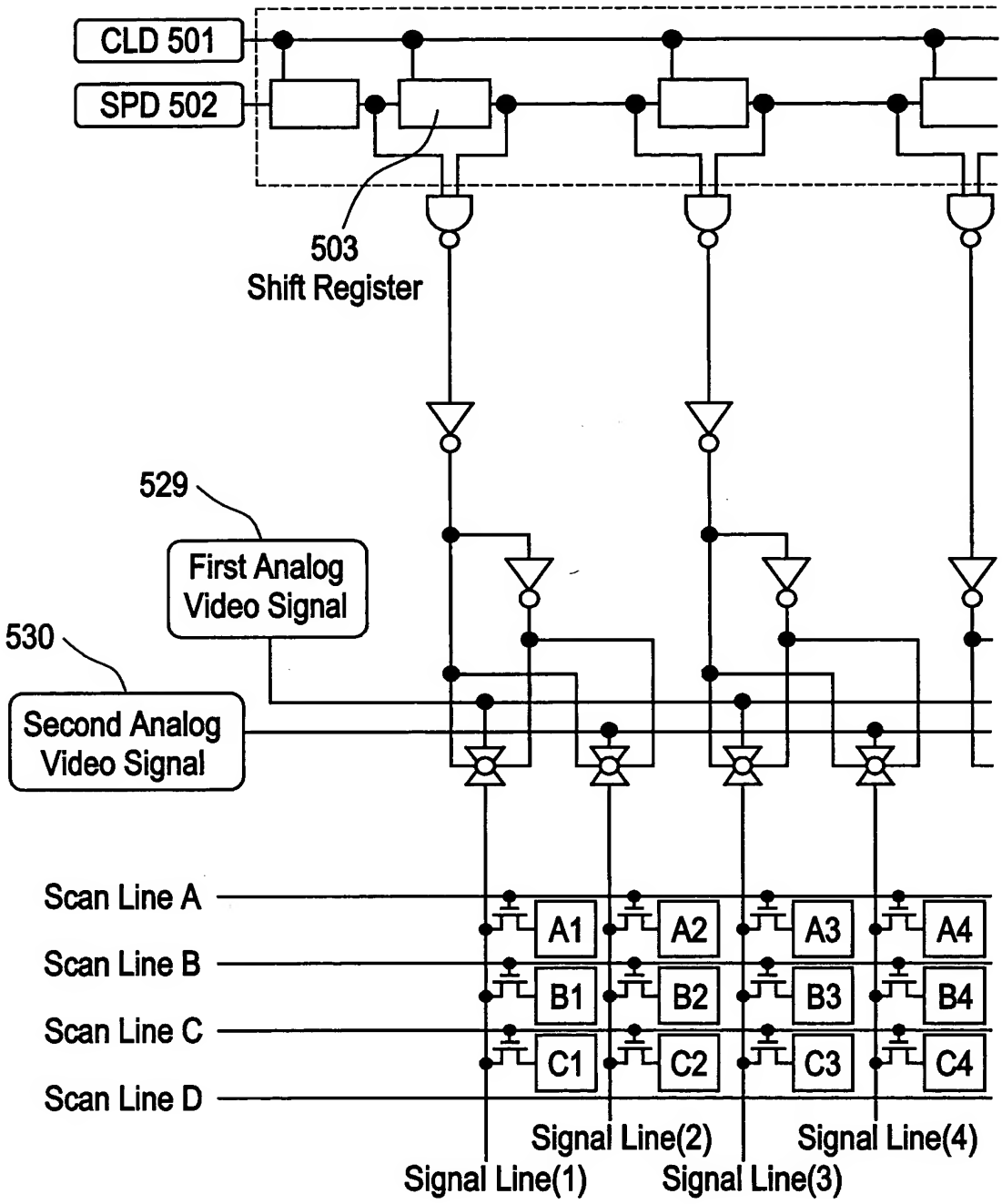


FIG.5B

Display Pattern

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4

FIG. 6

Rear Projection Type Display Device

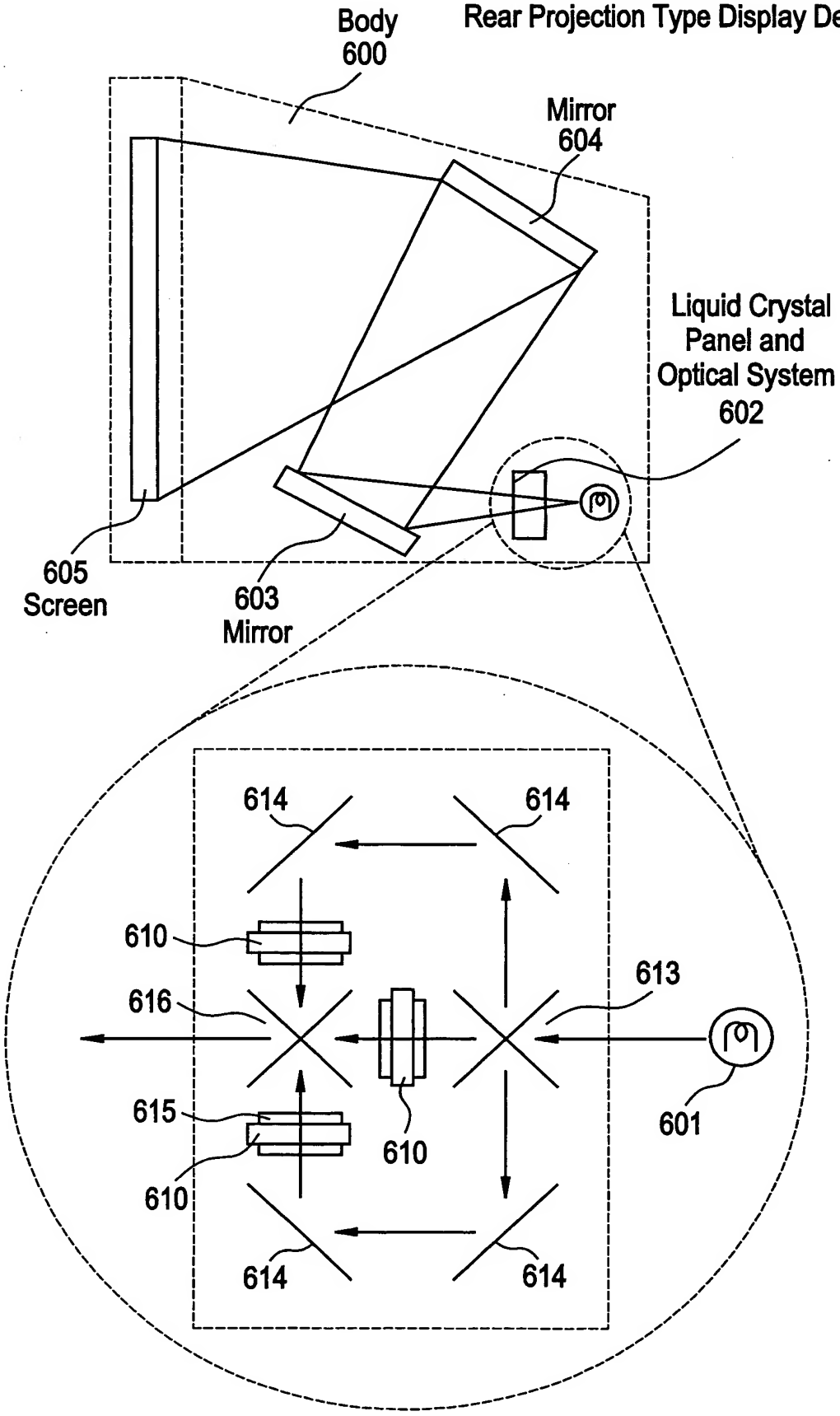


FIG. 7 PRIOR ART

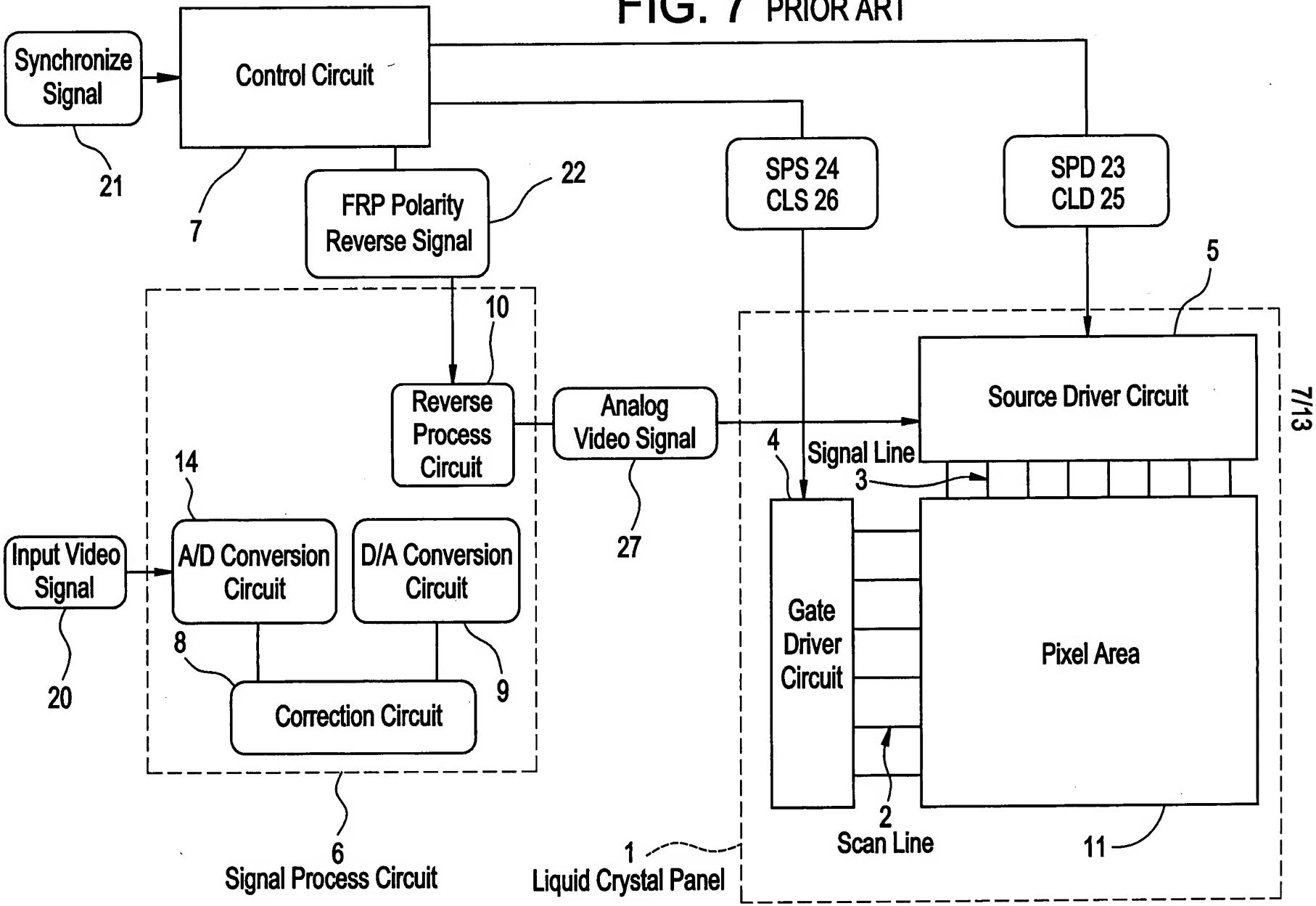


FIG. 8A

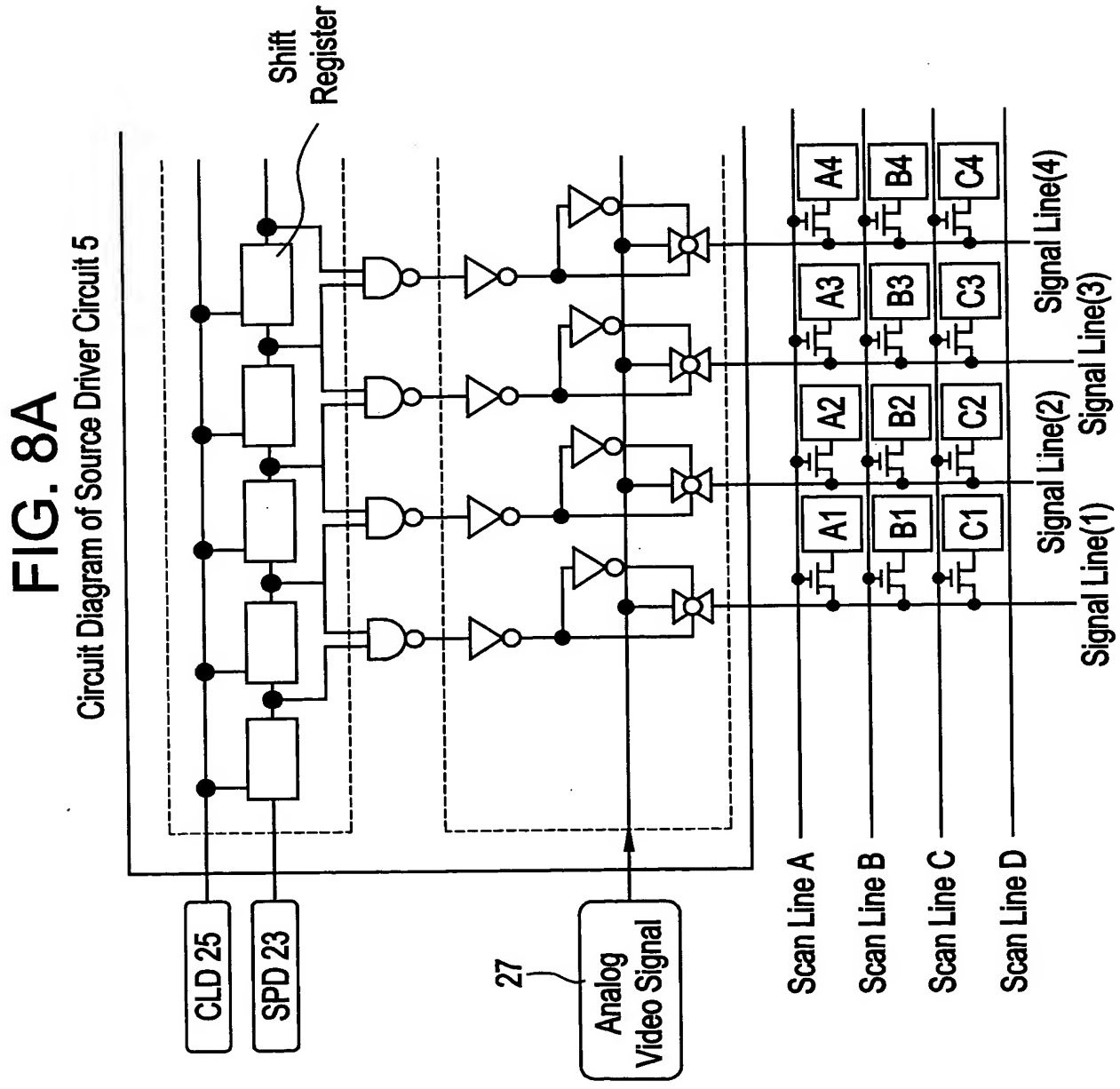


FIG. 8B

Display Pattern

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4

FIG. 9

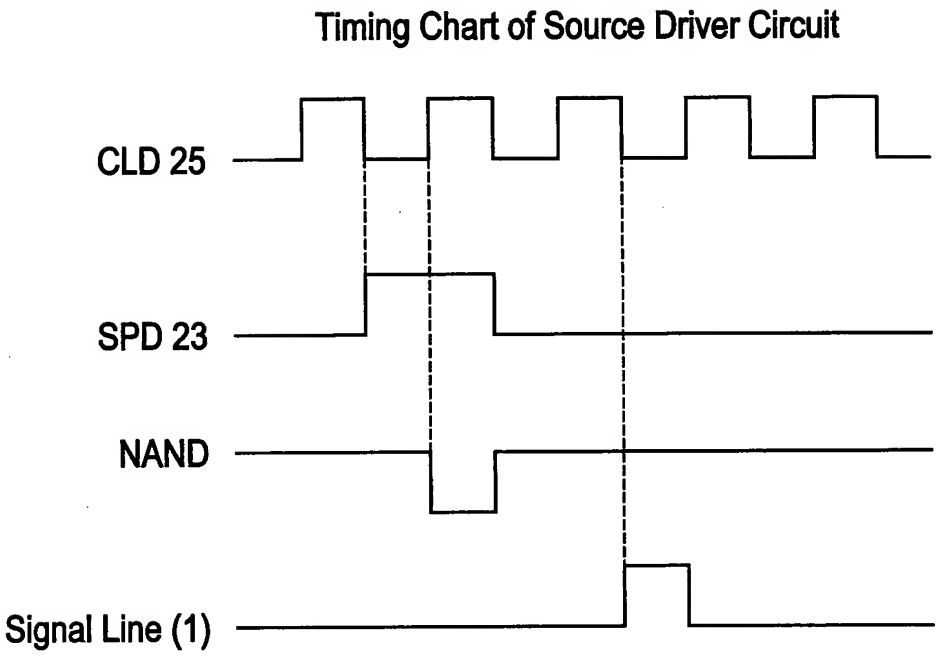

Timing Chart of Source Driver Circuit
CLD 25
SPD 23
NAND
Signal Line (1)

FIG. 10
PRIOR ART

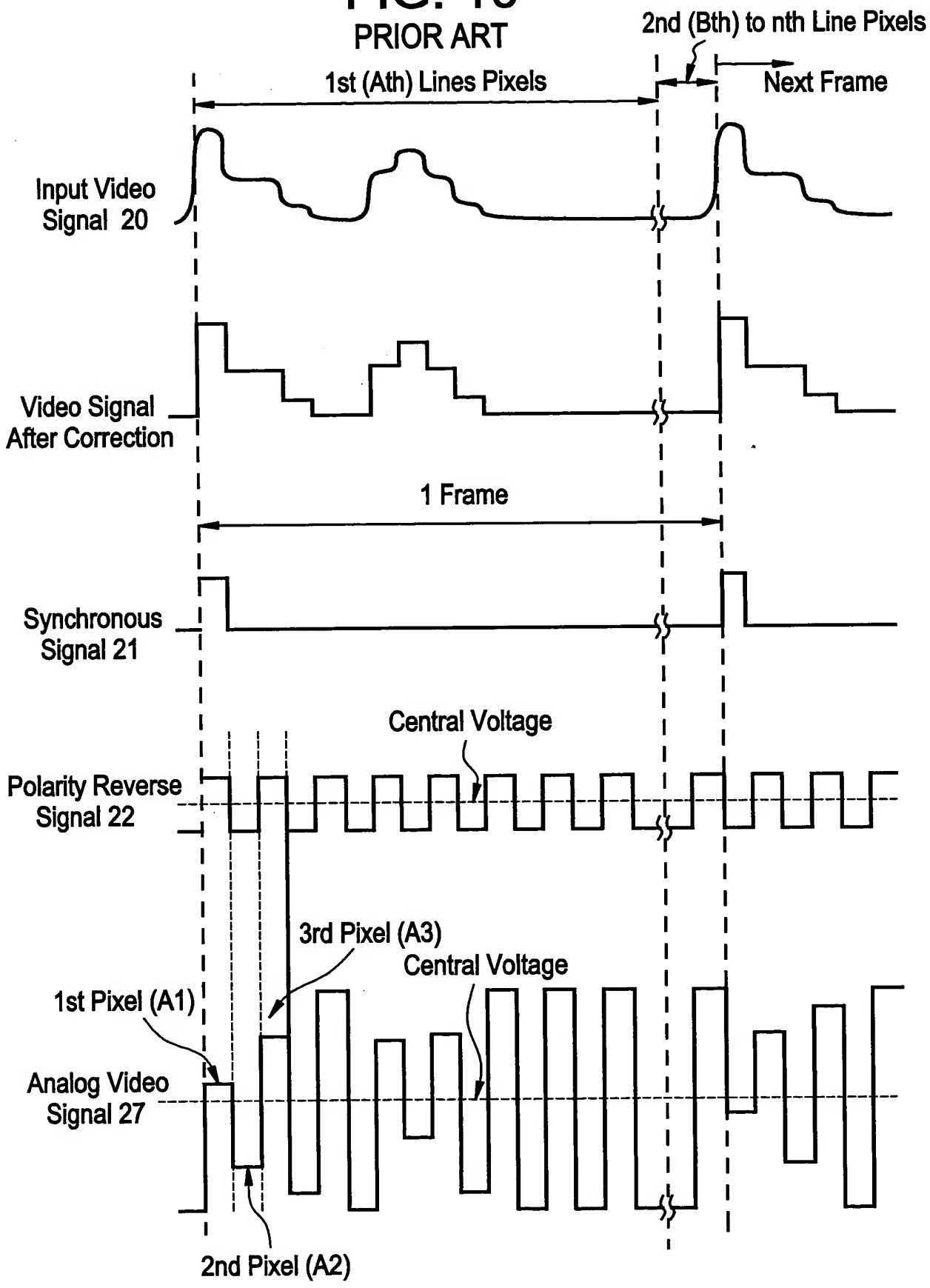


FIG. 11A

Display pattern

A1	A2	A3	A4	A5	A6
B1	B2	B3	B4	B5	B6
C1	C2	C3	C4	C5	C6
D1	D2	D3	D4	D5	D6
E1	E2	E3	E4	E5	E6
F1	F2	F3	F4	F5	F6

FIG. 11B

+	-	+	-	+	-
+	-	+	-	+	-
+	-	+	-	+	-
+	-	+	-	+	-
+	-	+	-	+	-
+	-	+	-	+	-

FIG. 11C

-	+	-	+	-	+
-	+	-	+	-	+
-	+	-	+	-	+
-	+	-	+	-	+
-	+	-	+	-	+
-	+	-	+	-	+

FIG. 12A

Display Pattern at Each Frame
Frame Inversion

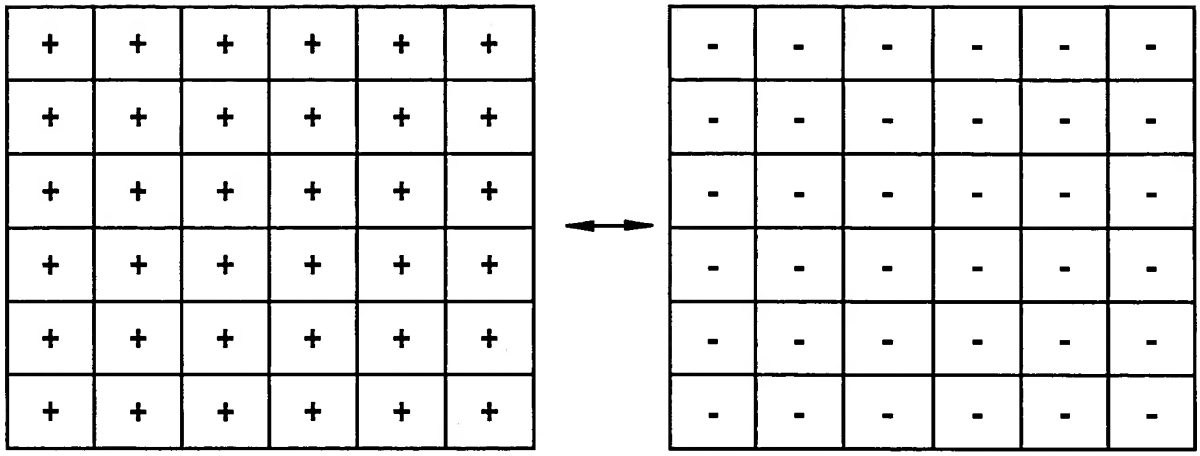


FIG. 12B

Gate Line Inversion

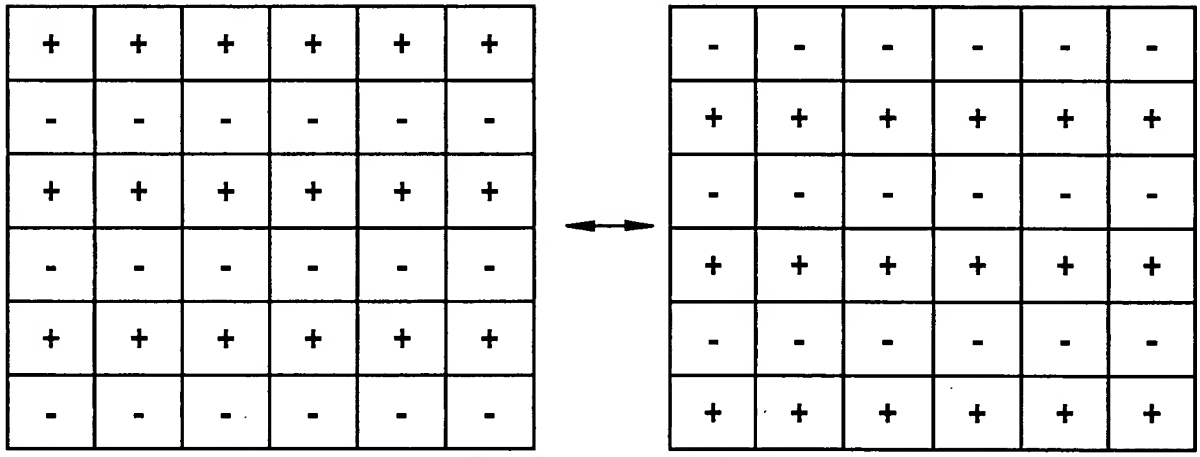


FIG. 12C

Dot Inversion

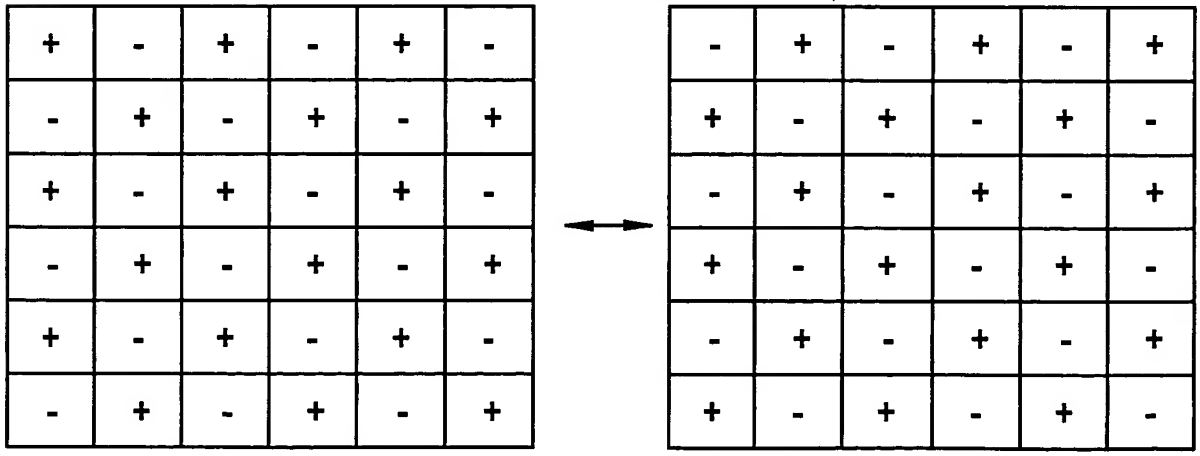
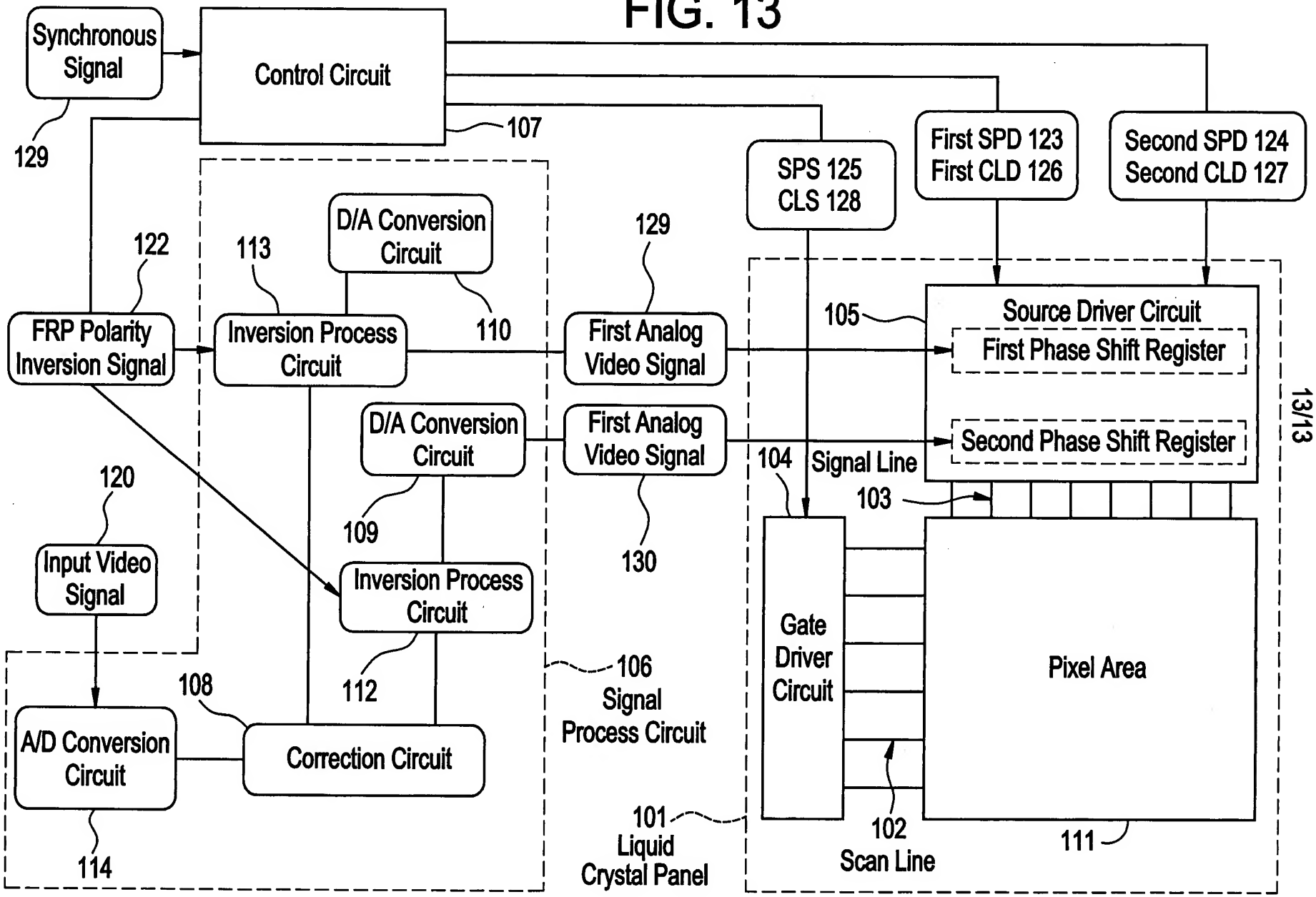


FIG. 13


Synchronous Signal
129
Control Circuit
107
SPS 125
CLS 128
First SPD 123
First CLD 126
Second SPD 124
Second CLD 127
122
FRP Polarity Inversion Signal
113
Inversion Process Circuit
D/A Conversion Circuit
110
129
First Analog Video Signal
105
Source Driver Circuit
First Phase Shift Register
Second Phase Shift Register
13/13
D/A Conversion Circuit
First Analog Video Signal
104
Signal Line
103
120
Input Video Signal
109
130
Inversion Process Circuit
112
106
Signal Process Circuit
Gate Driver Circuit
Pixel Area
108
A/D Conversion Circuit
Correction Circuit
114
101
Liquid Crystal Panel
102
Scan Line
111